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REPORT NO. 146

CABLE DRIVER AND TERMINATOR DESIGN

by

Shigeharu Yamada

August 21, 1963

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1. INTRODUCTION

This paper gives a theoretical treatment of a cable driver and cable terminator design of very general applicability. In general, problems of cable driver and terminator design separate into two parts:

(1) the noise problem, which includes both inter-channel crosstalk and the ground noise problem of coupling between different machines at different ground references;

(2) performance of the driver and terminator network, subject to prescribed level shifting, to give sufficient termination--including an allowable limit for reflection under the worst-case operation.

The first problem, ground noise, sometimes becomes considerable in magnitude, especially if a high-level system and a low-level system are connected. Obviously in AC systems ground noise can be suppressed by using a transformer to separate the longitudinal circuit coupling the two systems. In a DC system, a linear differential amplifier or a balanced transmission line can efficiently reject ground noise. On the other hand, from standpoint of economy a differential amplifier terminator is not preferable if ground noise can be held within allowable limits.

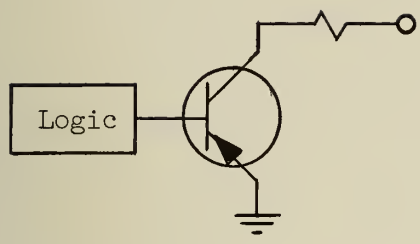
The second problem mentioned above can be summarized as the matching and level shifting problem. Cable impedance matching is not necessarily complete because of the nonlinear amplification of the terminator. (This situation will be discussed later.) A linear emitter follower driver and terminator are considered to give a better match at the sending and receiving ends, but level shifting is rather poor.

From the above circumstances, a driver and a terminator which give reasonable matching and complete level shifting are preferable in most digital applications. Such designs impose no additional level shifting circuitry at the stage preceding the driver and the stage succeeding the terminator. Accordingly, the driver and terminator can be connected directly to logic circuits without these intermediate stages.

These considerations suggest a suitably designed on-off driver and on-off terminator. Table 1 shows possible combinations of an on-off driver and

Driver

Terminator



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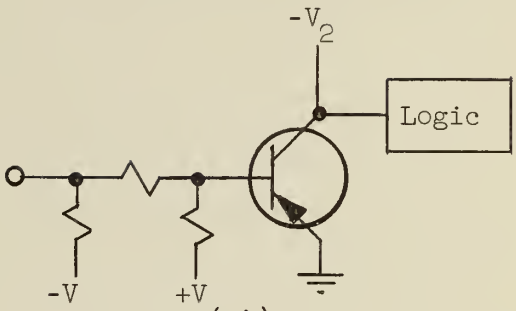

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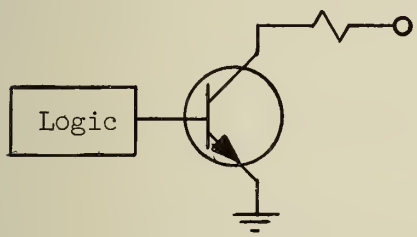

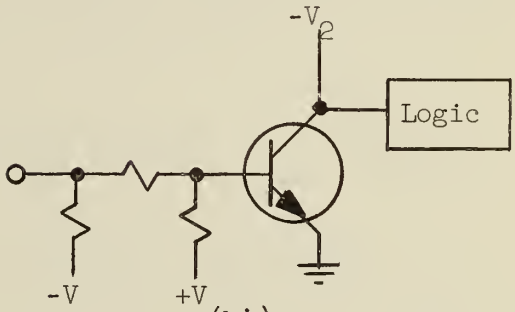

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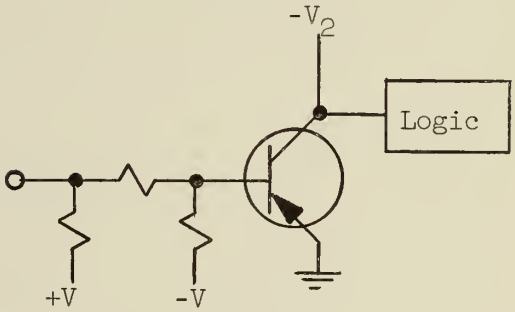

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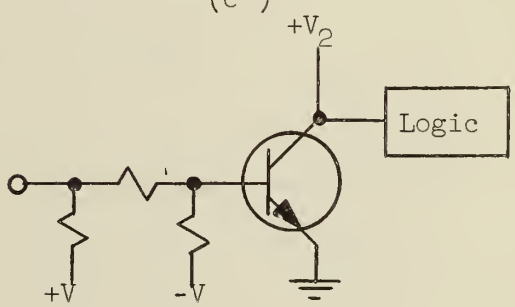

(d')

(a) → (a') $\begin{pmatrix} +V_1 \\ 0 \end{pmatrix}, \begin{pmatrix} 0 \\ -V_1 \end{pmatrix} \rightarrow \begin{pmatrix} 0 \\ -V_2 \end{pmatrix}$

(a) → (b') $\begin{pmatrix} 0 \\ -V_1 \end{pmatrix} \rightarrow \begin{pmatrix} +V_2 \\ 0 \end{pmatrix}$

(b) → (c') $\begin{pmatrix} +V_1 \\ 0 \end{pmatrix} \rightarrow \begin{pmatrix} 0 \\ -V_2 \end{pmatrix}$

(b) → (d') $\begin{pmatrix} 0 \\ -V_1 \end{pmatrix}, \begin{pmatrix} +V_1 \\ 0 \end{pmatrix} \rightarrow \begin{pmatrix} +V_2 \\ 0 \end{pmatrix}$

Table 1. Possible Combinations of Cable Driver and Terminator

an on-off terminator which give both noninverted information transmission and arbitrary level shift. These combinations work as a regenerative OR circuit and AND circuit in cooperation with the terminator.

Consider allowable limitation of the reflection for the driver-terminator pair. The limits on the reflected wave depends upon the delay time of the reflected wave from the main signal and upon the turn-on time of the terminator transistor. When the reflected wave comes after the completion of turn-on, the limits on the reflected wave will be less severe: once the transistor comes to a stable state, the reflected wave does not change the operating state unless

$$\min S(t) - |R(t) + N(t)| > \text{critical signal} \tag{1.1}$$

Here, critical signal means that signal level which breaks the saturated operation. Signal min $S(t)$ means that signal level which satisfies the lowermost operating condition. If α represents the ratio of the critical signal to the minimum signal, then the above equation gives

$$1 - \frac{|R(t) + N(t)|}{\min S(t)} > \alpha \tag{1.2}$$

Therefore, if α is designed to be $1/2$, this gives

$$|R(t) + N(t)| < 1/2 \min S(t) = 1/4\ \Delta S(t) \tag{1.3}$$

For the most part, min $S(t)$ is close to the $1/2$ of the signal level difference of the two stable states. On the other hand, if the reflected wave arrives before the completion of switching, the allowable limitation on the maximum reflected wave becomes more severe.

When the switching speed of the terminator is less than $2\ell/v$ (where v is the group velocity in the cable and ℓ is the length of the cable), the condition

$$\max |\delta S(t)| > |R(t) + N(t)| \tag{1.4}$$

must be satisfied. Here max $|\delta S(t)|$ is the allowable signal level variation which guarantees worst-case operation. This case is much more severe than the former case, but if the switching delay caused by reflection is allowed to a certain extent, the limitation of the reflection constraint is relaxed.

The operational equation which defines this delay is

$$1 - e^{-t} = (1 - e^{-T})F(p),$$

where

$$F(p) = \frac{1 + Re^{-2p\tau}}{1 - (-R)^{n+1}e^{-2(n+1)p\tau}} \qquad (1.5)$$

Here R is the ratio of the reflected wave to the signal and T is the relative build-up time (or fall time) without the presence of the reflected wave. τ is the cable delay. The delay depends both upon the reflected level and the cable delay time. Figure 1 shows the relative build-up delay caused by the reflection as calculated from Eq. (1.5).

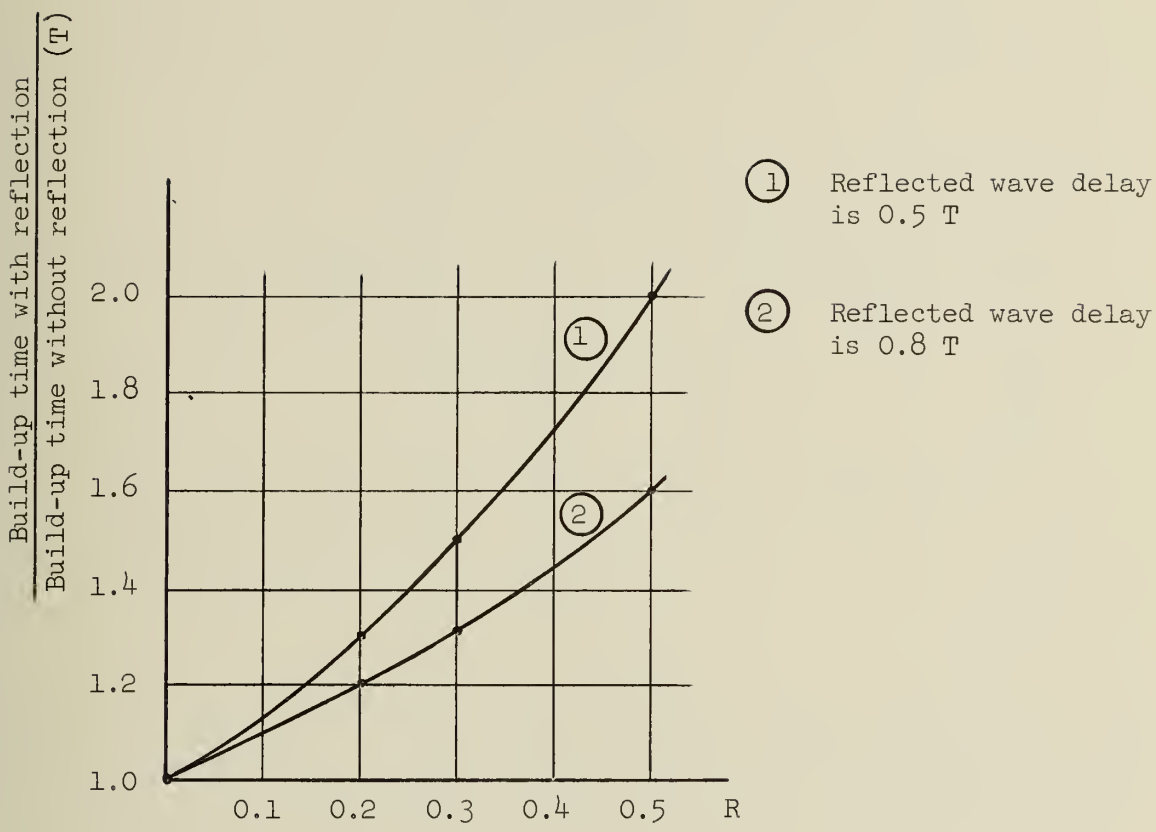

Figure 1. Ratio of Reflected Wave to Signal (R)

2. EQUATIONS AT EQUILIBRIUM

Consider the circuit shown in Fig. 2. This circuit can be expressed by the following equation (especially convenient for noise estimation):

$$\begin{pmatrix} e \\ j \end{pmatrix} = [A][V] + [B]\begin{pmatrix} v \\ i \end{pmatrix} \tag{2.1}$$

$$\begin{pmatrix} \Delta e \\ \Delta j \end{pmatrix} = [B]\begin{pmatrix} \Delta v \\ \Delta i \end{pmatrix}$$

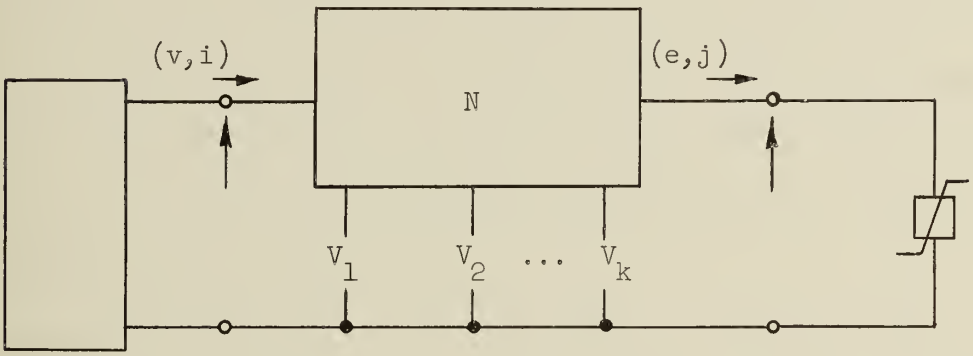

Figure 2

(V) does not depend upon the termination condition. [A] and [B] depend upon the circuit configuration. If the network is divided into cascaded subcircuits, each has an $[A_i]$, $[B_i]$ respectively. [A] and [B] can be expressed, as in the ordinary chain matrix, by the matrix of a subcircuit as follows:

$$[A] = \ldots [A_3] + [B_3][A_2] + [B_3][B_2][A_1]$$

$$[B] = \ldots [B_3][B_2][B_1] \tag{2.2}$$

Equation (2.1) should be solved for given input/output voltages and current conditions (these are given by the speed requirements of the regenerating transistor) and for given condition of input impedance, say,

$$Z_{in} = R_0,$$

$$\Delta Z_{in} = QR_0 \tag{2.3}$$

for one of two equilibrium conditions.

Network N is a passive linear circuit; therefore, the solution of Eq. (2.1) under the condition of Eq. (2.3) and given voltage and current conditions, must be positive.

Figure 3 shows a simplified structure. In this case the input circuit gives only the termination condition and there are no energy sources in the input circuit except for noise and the reflected wave. The input terminating condition gives the change in the output voltage and current. This structure is suitable for a cable drivers--terminator pair, because the cable terminator need not serve as an energy source for the driver; it sometimes causes trouble with the preceding stage of the driver.

Figure 4 is the simplest circuit topology of the form of Fig. 3 and also is a necessary and sufficient circuit for a level-shifting terminator. $\binom{V}{i}$ can be eliminated from Eq. (2.1) in this case:

$$\begin{pmatrix} e_1 \\ e_2 \end{pmatrix} = [A](V) + [Z] \begin{pmatrix} j_1 \\ j_2 \end{pmatrix} \tag{2.4}$$

Here [Z] is the output impedance matrix which corresponds to the input condition. The problem is to find the network from Eq. (2.1) or Eq. (2.4) subject to the condition of Eq. (2.3).

For the circuit of Fig. 4, the steady-state equation for the two input/output states, as indicated in Eq. (2.4), is

$$\begin{pmatrix} e_1 \\ e_2 \end{pmatrix} = \begin{pmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + \begin{pmatrix} Z_{11} & 0 \\ 0 & -Z_{22} \end{pmatrix} \begin{pmatrix} j_1 \\ j_2 \end{pmatrix} \tag{2.5}$$

Here (e_1, j_1) corresponds to the input switch open; (e_2, j_2) corresponds to the input switch closed.

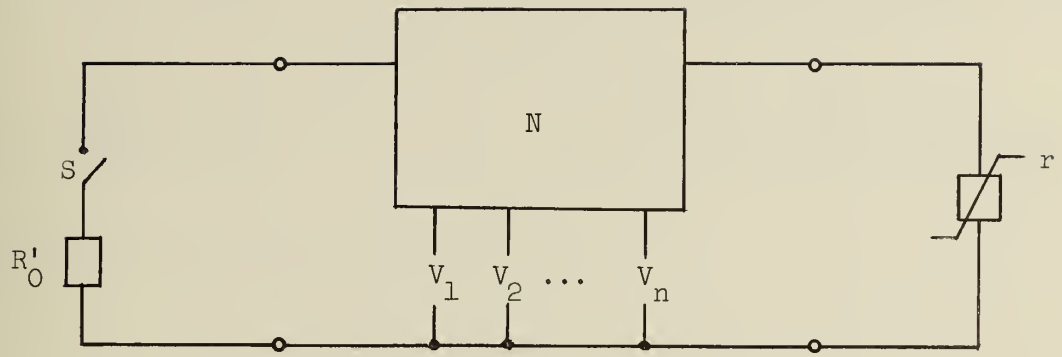

Figure 3

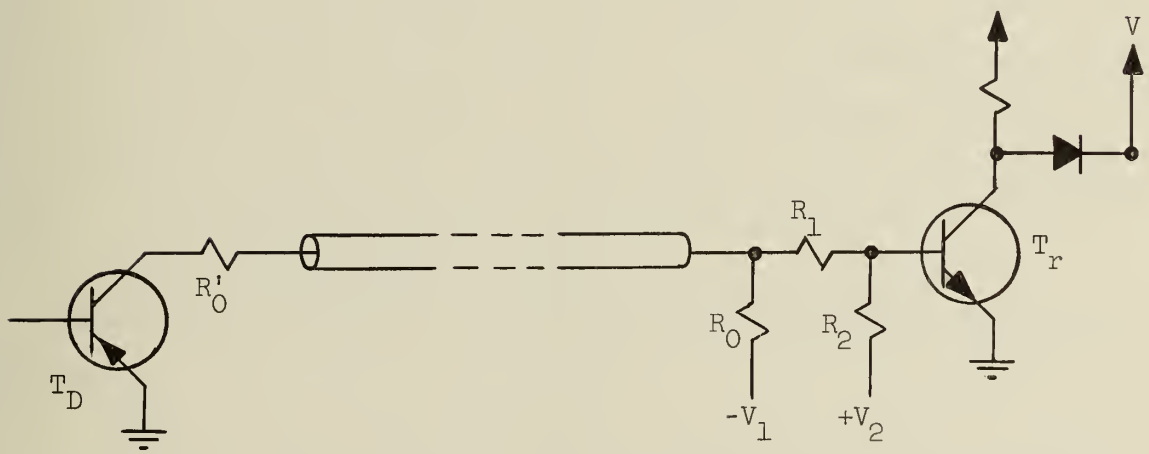

Figure 4

$$A_{11} = \frac{R_2}{R_0 + R_1 + R_2} \qquad A_{21} = \frac{R_0' R_2}{R_2(R_0 + R_0') + R_0'(R_0 + R_1) + R_0 R_1}$$

$$A_{12} = \frac{R_0 + R_1}{R_0 + R_1 + R_2} \qquad A_{22} = \frac{R_0'(R_0 + R_1) + R_0 R_1}{R_2(R_0 + R_0') + R_0'(R_0 + R_1) + R_0 R_1}$$

$$Z_{11} = \frac{R_2(R_0 + R_1)}{R_0 + R_1 + R_2} \qquad Z_{22} = \frac{R_2[R_1(R_0 + R_0') + R_0 R_0']}{R_2(R_0 + R_0') + R_0'(R_0 + R_1) + R_0 R_1}$$

The impedance condition for shorted T_r gives

$$\frac{R_0 R_0}{R_1 + R_0} = R_0'. \tag{2.7}$$

These equations determine R_0, R_1, R_2 for the given (e_1, j_1), (e_2, j_2) and V_1, V_2. Generally, to get the value of R_0, R_1, R_2, we must solve a set of higher order equations. When we limit the input impedance variation ΔZ_{in}, one of V_1 or V_2 cannot be given arbitrarily and the equation to be solved becomes of ths sixth order. For simplicity, in our case we omit the input impedance variation condition; therefore, V_1 and V_2 can be given arbitrarily within the limitation of the passive network approximation, and the equation reduces to a third order equation--or even a second order equation.

Equation (2.8) gives R_0 and R_1 as the function of R_2, e_1, e_2, j_1, j_2, V_1 and V_2;

$$R_0 = \left(\frac{V_1}{e_2} - 1\right) R_0' + 2R_0'\left(\frac{e_1}{e_2} - \frac{V_1}{e_2}\right)\left[1 + \frac{(e_1 - e_2) - R_2(j_1 + j_2)}{V_2 - e_1 + j_1 R_2}\right]$$

$$R_1 = \frac{R_2(e_1 - V_1)}{V_2 - e_1 + j_1 R_2} - R_0. \tag{2.8}$$

These two equations and Eq. (2.7) give an equation for R_2. If another impedance relation, which specifies the impedance condition where T_r is open, is added, the equation for R_2 becomes much more complicated. From Eq. (2.7) we get

$$A_0X^2 + A_1X + A_2 = 0 \qquad (2.9)$$

Another added impedance relation

$$\frac{R_0(R_1 + R_2)}{R_0 + R_1 + R_2} = QR'_0 \qquad Q > 1$$

gives a similar equation:

$$B_0X^2 + B_1X + B_2 = 0 \qquad (2.10)$$

where

$$X = V_2 - e_1 + j_1R_2,$$

$$A_0 = A_0(R_2^0) \qquad B_0 = B_0(R_2^1)$$

$$A_1 = A_1(R_2^1) \qquad B_1 = B_1(R_2^2)$$

$$A_2 = A_2(R_2^2) \qquad B_2 = B_2(R_2^2).$$

Equation (2.9) and Eq. (2.10) must have a common root; therefore, the condition (necessary and sufficient) is described by:

$$\begin{bmatrix} A_0 & 0 & B_0 & 0 \\ A_1 & A_0 & B_1 & B_0 \\ A_2 & A_1 & B_2 & B_1 \\ 0 & A_2 & 0 & B_2 \end{bmatrix} = 0 \qquad (2.11)$$

This gives a sixth order equation for R_2.

By solving Eq. (2.11) and substituting the root into X, V_2 can be determined. But this procedure is rather laborious; therefore we employ a

practical method which checks the input impedance variation only after getting a trial result, and if not satisfactory, revise the value of V_2 and recalculate. For example, if we put

$$V_1 = -6 \text{ volts} \qquad e_1 = -0.5 \text{ volts} \qquad j_1 = 0.1 \text{ ma}$$

$$V_2 = +6 \text{ volts} \qquad e_2 = +0.7 \text{ volts} \qquad j_2 = 1 \text{ ma}$$

then the equation for R_2 becomes

$$R_2^3 + 63.78\, R_2^2 - 77.98\, R_2 + 22.35 = 0 \tag{2.12}$$

This equation involves a trivial root; therefore, after factorization this becomes a second order equation, and gives the roots

$$R_2 = 0.7413 \text{ (K}\Omega\text{)}$$

$$R_1 = 0.4995 \text{ (K}\Omega\text{)}$$

$$R_0 = 0.1207 \text{ (K}\Omega\text{)} \tag{2.13}$$

These values show about 20 percent impedance variation. However, if we put $V_2 = +12$ volts, and the other conditions held to the same values as before, we get

$$R_2 = 2.676 \text{ (K}\Omega\text{)}$$

$$R_1 = 1.054 \text{ (K}\Omega\text{)}$$

$$R_0 = 0.09907 \text{ (K}\Omega\text{)} \tag{2.14}$$

In the latter case $\left|\frac{\Delta Z}{Z_0}\right|$ is less than six percent for the extreme case; this will be satisfactory.

So far, only mathematically accurate elements have been considered. In practice every element has tolerance variations. Consider now any circuit with all components having small variations but such that the behavior of the

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circuit can still be described completely by the analysis above. The worst case of the circuit behavior can then be described completely by an analytic method. On the other hand, if the circuit equation itself can be described only by statistical methods, even in a macroscopic view, we cannot describe the worst-case behavior by an analytic method. Another design philosophy of networks will be most economical: essentially a statistical design of circuits. Worst-case design sometimes gives uneconomical results. But such discussions are beyond the confines of this report. Therefore we will describe here only the determination of the worst-case equation. Assume, for convenience, that each element has small finite variations. Cross-terms of the variations can then be neglected when estimating the incremental change.

A worst-case equation corresponding to Eq. (2.5) becomes

$$\begin{pmatrix} e_1 \\ e_2 \end{pmatrix} = [A_{(1\pm\epsilon)}][V_{(1\pm\eta)}] + [Z_{(1\pm\delta)}]\begin{pmatrix} j_1 \\ j_2 \end{pmatrix} \tag{2.15}$$

Here $[A_{(1\pm\epsilon)}]$, $[V_{(1\pm\eta)}]$, and $[Z_{(1\pm\delta)}]$ represent matrices, the elements of which are multiplies by $(1 + \epsilon)$, $(1 - \epsilon)$, etc. The signs of ϵ, δ, η are determined by the sign of the partial derivative. $\frac{\partial j}{\partial e}$ is always positive. Therefore, to determine the appropriate sign of a variation, it is sufficient to check the sign of the partial derivative of e. Equation (2.5) and Eq. (2.6) give

$$\frac{\partial e_1}{\partial V_1} > 0, \quad \frac{\partial e_1}{\partial V_2} > 0, \quad \frac{\partial e_1}{\partial R_0} > 0, \quad \frac{\partial e_1}{\partial R_1} > 0$$

$$\frac{\partial e_1}{\partial R_2} < 0, \quad \frac{\partial e_2}{\partial R_0'} < 0. \tag{2.16}$$

The circuit parameters for the equation e_1, therefore, should be incremented as follows:

$$V_1 \to V_1(1 - \epsilon) \qquad R_0 \to R_0(1 + \eta) \qquad R_2 \to R_2(1 - \eta)$$

$$V_2 \to V_2(1 + \epsilon) \qquad R_1 \to R_1(1 + \eta) \tag{2.17}$$

Correspondingly we have for the equation e_2:

$$V_1 \to V_1(1+\epsilon) \qquad R_0 \to R_0(1-\eta) \qquad R_2 \to R_2(1+\eta)$$

$$V_2 \to V_2(1-\epsilon) \qquad R_1 \to R_1(1-\eta) \qquad R_0' \to R_0'(1+\eta) \qquad (2.18)$$

Now, if we give (e_1, j_1) for the condition (2.17) and give (e_2, j_2) for the condition (2.18), we find we cannot assign arbitrarily (e_2, j_2) for condition (2.17) and (e_1, j_1) for condition (2.18), because there are more conditions than degrees of freedom of the circuit. (e_1, j_1) under the condition of (2.17) determines the maximum level of the cutoff. (e_2, j_2) for the condition (2.18) determines the minimum level of the saturation. On the other hand (e_1, j_1) for the condition (2.18) gives the minimum level of the cutoff, and (e_2, j_2) for the condition (2.17) gives the maximum level of the saturation. These latter two values should be deduced from the former two values, but the interrelation of these values are not defined until the equation is solved. Therefore, the equation for worst-case operation for specified input impedance can be given, not by a straightforward method, but only by an iterative procedure.

Equations (2.5), (2.6) and (2.7), modified by the condition (2.17) and (2.18), give a third order equation of R_2. R_2 cannot always be realizable for preselected voltage and current levels, given percentage variation of circuit elements, and given impedance condition. If we ignore the impedance condition, as for the case of ordinary logical circuits, the worst case equation is deduced much more easily. In our case, in addition to the passive condition, another realizability condition (a sufficient condition) must be met:

$$\left.\begin{array}{c} Q_1 < 0 \\ \text{and} \\ Q_2 R_2^2 + 2Q_1 R_2 + 3Q_0 < 0 \\ \text{for the root of the equation,} \\ 3Q_3 R_2^2 + 2Q_2 R_2 + Q_1 = 0 \end{array}\right\} \qquad (2.19)$$

where Q_0, Q_1, Q_2, Q_3 are the corresponding coefficients of R_2^0, R_2^1, R_2^2, R_2^3.

If Eq. (2.19) cannot be satisfied for given initial conditions, these conditions must be changed until they satisfy Eq. (2.19). The following is an example:

$V_1 = -6$ volts $\pm$ 5% $\quad e_1 = -0.3$ volts $\quad j_1 = 20$ μa

$V_2 = +12$ volts $\pm$ 5% $\quad e_2 = +0.8$ volts $\quad j_2 = 1$ ma

R_0', R_0, R_1, R_2 vary $\pm$ 5%

input impedance for saturation termination = 91Ω $\pm$ 5%

For these conditions, equation of R_2 becomes

$$R_2^3 + 579.7955\ R_2^2 - 1658.870\ R_2 + 1049.5538 = 0 \qquad (2.20)$$

and satisfies the condition (2.19). The solutions are:

$R_2 = 1.9043$ (KΩ)

$R_0 = 0.1059$ (KΩ)

$R_1 = 0.6493$ (KΩ)

These values give about 5% impedance variation when T_r is in either the short or open condition.

Cable transmission loss enters through the variation of the resistance R_0'. The practical values of R_0, R_1, R_2 will be:

$R_2 = 1.8$ KΩ, 5%

$R_0 = 100$Ω, 5%

$R_1 = 650$Ω, 3% (will be selected from 680Ω, 5%)

Practical configurations and data are reported in a separate paper.*

* S. Yamada and D. Foster, Data on Cable Drivers and Terminators for ILLIAC III, Digital Computer Laboratory, File No. 565, August, 1963.

3. TRANSIENT CONSIDERATIONS

The aim of this section is to investigate the nonlinear influence on the wave form at the input of the terminator.

Consider the circuit of Fig. 4. This is equivalent to the circuit of Fig. 5 if the ground potential problem is neglected. Z_0 and V_0 are the equivalent impedance and supply voltages respectively. V_0 and Z_0 vary accordingly as the input switch changes and can be represented as a function of time t and e_2. Assume now that these changes are rather slow compared to the operation of the switch.

For the first case, consider the switch open at $t < 0$, and closed at $t = 0$. e_2 equals $e_2'(t) + V_0(t)$; e_2' is the voltage change at the terminal (2, 2') which is caused by the voltage change at (1, 1'). Consider now a small time interval T. For this interval, the circuit is assumed to be linear.

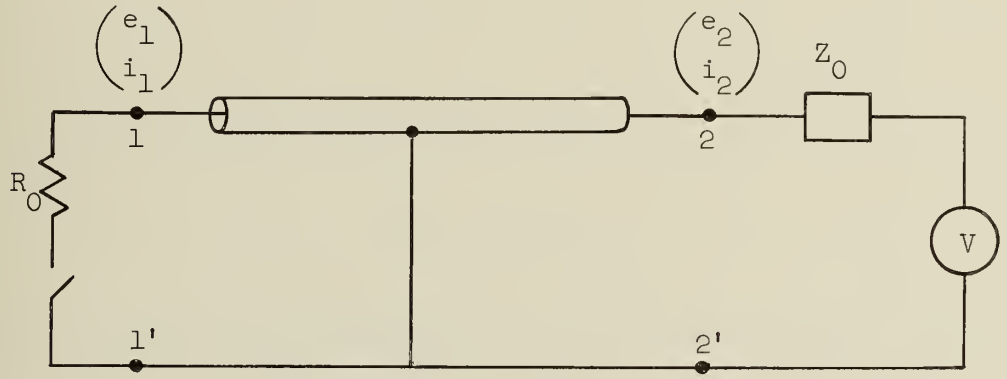


Figure 5

The equation of the circuit, neglecting cable loss, becomes:

$$\begin{pmatrix} e_1 \\ i_1 \end{pmatrix} = \begin{pmatrix} \cosh p\tau & R_0 \sinh p\tau \\ R_0^{-1} \sinh p\tau & \cosh p\tau \end{pmatrix} \begin{pmatrix} e_2' \\ i_2 \end{pmatrix} \qquad (3.1)$$

$$e_1 = -V_0(t) - i_1 R_0$$

For a first approximation, $V_0(t)$ is taken as a staircase function, that is

$$V_0(t) = \sum_i \int_{t-t_i}^{t-t_{i+1}} V(t_i)\delta(t - t_i)dt \qquad (3.2)$$

The successive values of $V(t_i)$ converge to the equilibrium value. From Eqs. (3.1) and (3.2), we obtain

$$e_2(t) = -\frac{V_0(t - T)}{2} e^{-p\tau}\left[1 \pm \frac{R(\dot{\xi})}{2R_0}\right] + V_0(t - T) \mp \frac{I(\dot{\xi})}{2R_0}\frac{d}{dt} V_0(t - T)e^{-p\tau}$$

for

$$t < \tau + T$$

where

$$\dot{\xi} = R(\dot{\xi}) \pm pI(\dot{\xi})$$

$$Z_0 = R_0 + \dot{\xi} \qquad (3.3)$$

For $\tau > T$ the equivalent source voltage $V_0(t)$ increases successively, and $Z_0(t)$ decreases. These changes add together. The circuit design in the preceding section satisfies

$$\delta V_0(t) = \frac{\delta Z_0}{R_0} V_1$$

for the first approximation. Therefore, the voltage change at the input of the terminator is equal to

$$\frac{-\delta Z_0}{2R_0} V_0 + \delta V_0 = \frac{\delta Z_0}{2R_0} V_0$$

This change shows the increase of voltage for a given magnitude of impedance variation.

By the same method as above, $e_2(t)$, which corresponds to the switch suddenly opened, can be calculated. In this case, instead of inserting a voltage source, we insert a current source:

$$\frac{V_0(t)}{R_0 + Z_0} \equiv I(t)$$

at the place of switch. Therefore, $e_2(t)$ becomes

$$e_2(t) = V_0(t - T) - \frac{V_0(t - T)}{2} \frac{1 \pm \frac{R(\dot{\xi})}{R_0}}{1 \pm \frac{R(\dot{\xi})}{2R_0}} + \frac{V_0(t - T)}{2} \frac{1 \pm \frac{R(\dot{\xi})}{R_0}}{1 \pm \frac{R(\dot{\xi})}{2R_0}} \frac{e^{-p\tau}}{1 \pm \frac{R(\dot{\xi})}{2R_0}(1 - e^{-2p\tau})} \tag{3.4}$$

for

$$t < T + \tau .$$

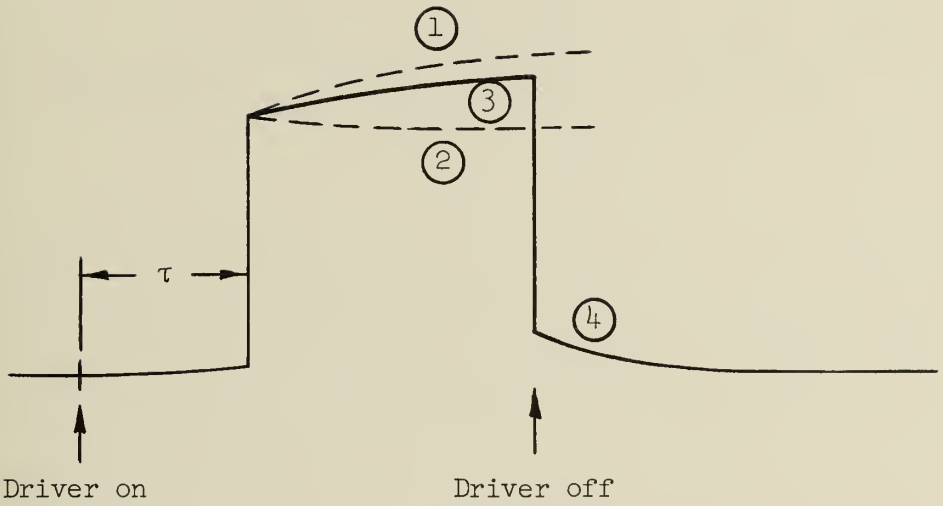
$V_0(t)$ is again the staircase function for $t > T + \tau$ and is also determined by the resistance characteristics of the transistor and e_2. For $t > T$, by the same observation as before, $e_2(t)$ decreases to the equilibrium voltage. These results are shown in Fig. 6.

Equation (2.3) represents multiple reflections; the first reflected wave, delayed by 2τ from the main signal, is

$$\pm \frac{R(\dot{\xi})}{2R_0} V_0(t) \pm \frac{I(\dot{\xi})}{2R_0} \frac{dV_0(t)}{dt}$$

In both cases, if the imaginary part of $\dot{\xi}$ (which is essentially wiring inductance or parasitic capacitance) is small, the wave form distortion depends mainly upon the characteristics of the terminating transistor.

The above analysis shows the equilibrium level is higher in absolute magnitude both in the switch-on and switch-off cases; it is better to take into account these situations for a worst-case design.



① δe_2 caused by $\delta V_0(t)$

② δe_2 caused by δZ_0

③ ① + ②

④ δe_2 caused by $\delta V_0 + \delta Z_0$

Figure 6. Dependence of $e_2(t)$ on Variations of V_0 and Z_0

4. NOISE PROBLEMS

Noise problems which arise when two computers are connected are sometimes very complicated. Noise is composed of two parts. One part is noise from adjacent channels through direct coupling between wires; the other part is noise from the ground circuit. The noise ratio of the former can be expressed by

$$\sum_n \int_0^{\ell} \left(\frac{Zmn(x)}{R_0} - Ymn(x)R_0 \right) e^{-\frac{j\omega\ell}{v}} dx + \sum_n \int_0^{\ell} \left(\frac{Zmn(x)}{R_0} + Ymn(x)R_0 \right) e^{-\frac{2j\omega x}{v} - \frac{j\omega\ell}{v}} dx \tag{4.1}$$

The first term represents the direct noise to the receiving end, and the second term represents the reflected noise at the sending end. Ordinary Zmn's, Ymn's are reactances; therefore, the wave form of the noise has a pulse shape. This can be easily shown by the Laplace transformation of Eq. (4.1).

The second term of Eq. (4.1) shows the distributed pulse train along the time axis, which length corresponds to the pass length of the noise. For coaxial cable, Zmn, Ymn are small. This can be checked by experiment.

The second noise contribution arises from the mechanism shown in Fig. 7. When we use a transformer, longitudinal pass can be shut off; of if we use a balanced system it can be eliminated. Otherwise this kind of noise cannot be eliminated.

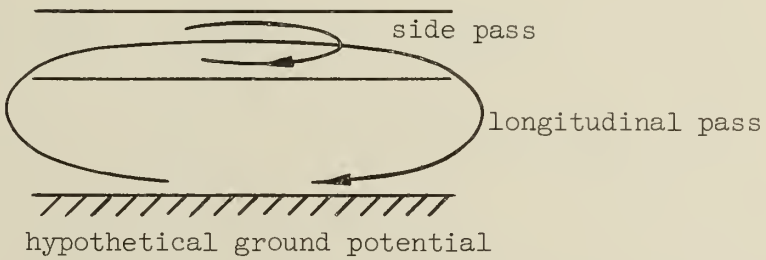


Figure 7

Estimation of the noise is as follows. Let V_1, V_2, I_1, I_2 be the potential differences and the currents referred to the hypothetical ground potential. Translate these potential differences and currents by matrix [S],

$$[S] = \begin{bmatrix} 1 & -1 \\ \frac{1}{2} & \frac{1}{2} \end{bmatrix},$$

where now

$$[e] = [S] \cdot [V]$$

$$[i] = [S] \cdot [I] \qquad (4.2)$$

The equation of the transmission line is

$$\begin{pmatrix} e_1 \\ i_1 \end{pmatrix} = \begin{pmatrix} \cosh [\Gamma]\ell & w_0 \sinh [\Gamma]\ell \\ w_0^{-1} \sinh [\Gamma]\ell & \cosh [\Gamma]\ell \end{pmatrix} \begin{pmatrix} e_2 \\ i_2 \end{pmatrix}$$

The matrix $[\Gamma]$ may be considered diagonal, but w_0 is not a diagonal matrix.

$$[V] = [Z] \cdot [I] \qquad [Z]^* = [Z]$$

$$[z] = S[Z]S^{-1}$$

$$w_0 = [\Gamma]^{-1} \cdot [z]$$

$$W_0 = \begin{pmatrix} \left(\frac{Z_{11} + Z_{22}}{2} - Z_{12}\right)\frac{1}{\gamma_1} & (Z_{11} - Z_{22})\frac{1}{\gamma_1} \\ \frac{1}{4}(Z_{11} - Z_{22})\frac{1}{\gamma_2} & \left(\frac{Z_{11} + Z_{22}}{2} + Z_{12}\right)\frac{1}{\gamma_2} \end{pmatrix} \qquad (4.4)$$

Therefore, if $Z_{11} = Z_{22}$, the longitudinal pass and the side pass are independent of each other, and of course no noise occurs. But for an unbalanced cable this cannot be satisfied, while, in the balanced cable Z_{11} is equal to Z_{22}. Therefore in this latter case there exists very little longitudinal noise.

Equation (4.2) also illustrates this situation when $V_1 = -V_2$ (i.e., balanced transmission); there exists no longitudinal crosstalk. In any case

from the above considerations a pair cable will give better isolation from longitudinal noise.

Figure 8 shows the measurement of ground noise.

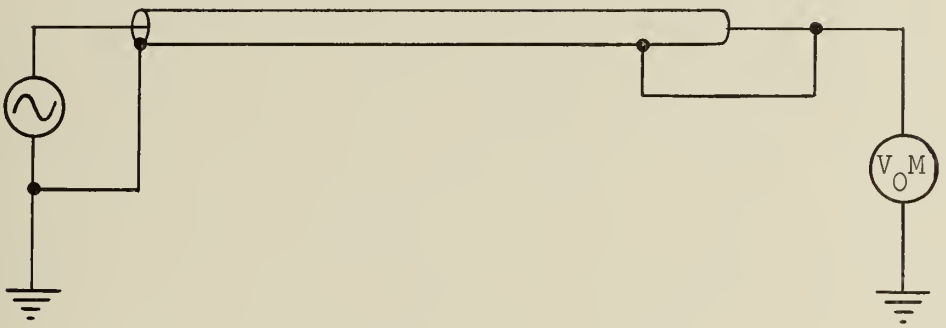


Figure 8. Measurement of Ground Noise

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